New Direction
New Markets
New Opportunities
• **FirmASIC®** is a CML proprietary technology that has been successfully deployed in a wide range of standard and custom product offerings. Key benefits of this technology include fast time-to market, low cost, low risk, small footprint and unsurpassed flexibility.

• **FirmASIC®** provides the optimum combination of analogue, digital, firmware and memory technologies in a single platform. A growing family of approved and stable hardware platforms is available, each providing a different mix of fixed and re-definable functions.

• The whole essence of **FirmASIC®** is delivering a product with the right feature mix, performance and cost for a specific target application, in the shortest possible time.
Custom Product Direction
Opening up new markets and expanding our mutual business

- New business direction complementing CML’s standard product line
- Opening up new markets
- Developing new product opportunities
- Targeting key manufacturers
  - Wireless communications
  - Wireline communications
  - Industrial control
  - Security systems
- Displacement strategy for ASIC, FPGA and DSP
- FirmASIC® technology has been used successfully in a number of standard, custom and semi-custom CML product offerings
- The FirmASIC® approach is ideally suited to the European business model
Key Benefits

- Fast time-to-product
  - No multiple silicon runs
  - Evaluation samples in typically 3 months
- Highly flexible
  - Family of hardware platforms each with different functions
  - Standard Function Image™ library
  - Custom functions
- Low cost
  - Reasonable NRE costs (Custom/Semi-custom)
  - Competitive end product costs
  - Realistic option for opportunities down to 50k units per annum
- Low risk
  - Stable hardware platforms
  - Evaluation stages allowing customer field trials
- Low power operation
  - The heart of the hardware platforms
- Small package footprint
## FirmASIC® Has The Edge

World leading ASIC, FPGA, and DSP replacement technology

<table>
<thead>
<tr>
<th>Advantage</th>
<th>ASIC</th>
<th>Gate Array</th>
<th>FPGA</th>
<th>DSP</th>
</tr>
</thead>
<tbody>
<tr>
<td>External + Internal NRE Costs</td>
<td>High</td>
<td>Tooling: Low</td>
<td>Tooling: Zero</td>
<td>Tooling: Zero</td>
</tr>
<tr>
<td>End Production Cost</td>
<td>Low</td>
<td>Low</td>
<td>Very High</td>
<td>Low</td>
</tr>
<tr>
<td>Time To Production</td>
<td>Long</td>
<td>Medium</td>
<td>Medium</td>
<td>Long</td>
</tr>
<tr>
<td>Cost to Add/Change Features</td>
<td>High</td>
<td>Medium</td>
<td>Medium</td>
<td>Low/Medium</td>
</tr>
<tr>
<td>Field Upgrade</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Market Specific Analogue Functions</td>
<td>Yes</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>Size</td>
<td>Small</td>
<td>Large</td>
<td>Large</td>
<td>Large</td>
</tr>
</tbody>
</table>

Legend:
- **Tooling**: Low (Zero), Medium (High)
- **Other**: Low (High)
- **Time To Production**: Long (Medium), Short (Low)
- **Cost to Add/Change Features**: High (Medium), Low/Medium (Low/Zero)
- **Field Upgrade**: No (Yes)
- **Market Specific Analogue Functions**: No (Yes)
- **Size**: Small (Large)

---

FirmASIC®: Has The Edge

Advantage

- **Tooling**: Low (Zero), Medium (High)
- **Other**: Low (High)
- **Time To Production**: Long (Medium), Short (Low)
- **Cost to Add/Change Features**: High (Medium), Low/Medium (Low/Zero)
- **Field Upgrade**: No (Yes)
- **Market Specific Analogue Functions**: No (Yes)
- **Size**: Small (Large)
Stable Hardware Platforms
The key to low risk low risk

- A family of hardware platforms are available
- Each has different embedded subsystems
- All have an analogue interface
- Low power operation
- Platforms generally have two offerings
  - RAM based for evaluation and early production
  - ROM based for series production
- 6 platforms are available
  - Platform 3, 4, 5, 6, 7 and 8
• **Wireless modem schemes**
  – FFSK/MSK, GMSK/GFSK, C4FM, 4FSK, 8FSK
• **Coding systems**
  – Interleaving, FEC, CRC
• **Wireline modems schemes**
  – V.32bis, V.32, V.22bis, V.22/Bell 212A, V.23/Bell 202, V.21/Bell 103
• **Signalling**
  – Audio band and sub-audio band signalling
  – Programmable single tone, DTMF, call progress tones, CLI, CIDCW, CTCSS, DCS, XTCSS
• **Audio processing**
  – Filtering, AGC, companding, scrambling, pre/de-emphasis, soft limiting
• **Signal measurement**
  – Threshold detection, averaging, hysteresis
• **Filtering**
  – Comprehensive range of digitally implemented filters
• **Custom Functions**
  – Application specific, user defined, designed to order
FirmASIC® - SoC Possibilities
World leading ASIC, FPGA, and DSP replacement technology

Applications

- ASIC, DSP, Structured ASIC and FPGA replacement
- SoC applications
- Embedded solutions
- Unlimited applications
  - Wireless
  - Wireline
  - Sensors
  - Industrial control
  - Security
  - .............

Typical System Application

- Host Microcontroller
- Serial Flash NV Data Storage
- Program Flash
- Analogue Input/Output Interface
- Signal Conditioning
- Auxiliary ADCs
- Clock Management
- Audio Codec
- Auxiliary Synthesised Clock O/Ps
- Auxiliary DACs
- Power Management
- Auxiliary GPIO
- Program Memory
- FPGA/ASIC/DSP
- SRAM

FPGA/ASIC/DSP

CML Microcircuits
COMMUNICATION SEMICONDUCTORS
Working with **FirmASIC®**

From definition through to delivered IC

**Project Flow**

- **Definition Phase**
  - Clear understanding of the requirement, operating definition
  - And parametric specification

- **Customer Evaluation Phase**
  - Evaluation board supplied containing the custom Function Image™ in onboard serial Flash

- **Development Phase**
  - Utilising CML’s function library and construction of custom functionality

- **Customer Evaluation Phase**
  - Evaluation board supplied containing the custom Function Image™ in onboard serial Flash

- **Customer Preproduction**
  - RAM based product available Function Image™ retained in serial Flash

- **Product Production Release**
  - Custom mask product availability
Platform 4
Field proven hardware

Analogue Signal Processing

Platform 4

CML Signal Processing Engine

Processing Channel 1

Processing Channel 2

Auxiliary Systems

DAC 1

ADC 1

ADC 2

DAC 1

Sample Input 1

Sample Input 2

Sample Input 3

Synthesised clock 1

Synthesised clock 2

GPIO

RAM

Subsystem Function Library

Boot configuration

PLL

Power Management

Power Supply and Bias Generator

CML Microcircuits
COMMUNICATION SEMICONDUCTORS
Platform 3
Field proven hardware
### FirmASIC® Approach

**Product definition and contract**

**Product design and development completed and RAM based evaluation released**

**Customer field trials and approval**

**Semi-custom RAM based product available**

**Custom early/pre-production can start**

**Custom ROM based devices supplied**

### Case Study

**Utility meter radio control processor (SoC)**

- **Company looking to commission a new ASIC to replace existing ASIC due to concerns about process availability**

- **Opportunity qualified, FirmASIC® route chosen and feasibility study completed**

- **Scope and contract**

- **Design and Tooling**

- **Evaluation & Field Trials**

- **Semi-custom RAM based product available**

- **Custom early/pre-production can start**

- **Custom ROM based devices supplied**

### Typical Custom ASIC Route

| Months | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 |
|--------|---|---|---|---|---|---|---|---|---|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|       |   |   |   |   |   |   |   |   |   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
Product Support
Fast efficient evaluation kit and IC

Evaluation

PE0002
Universal interface card

PE0201

PE0401

PE0501

USB
C-BUS
• Completely new design approach
• Target market is ASIC, FPGA, and DSP replacement
• Embedded auxiliary functions
• Analogue and digital functionality on chip
• Fast time-to-production
• Highly flexibility
• Low risk
• Low cost
• SoC capability